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Low Power VLSI for Bio-Medical Application

Akarsha Ram[1], *Aakash M*[1], *Sivakumar R*[1*]

[1]*School of Electronics Engineering (SENSE), Vellore Institute of Technology, Vellore, India*

[*]*Corresponding author's Email: rsivakumar@vit.ac.in*

Introduction

Cardiac Pacemakers are a set of implantable devices used to generate rhythm for slow beating hearts. The application requires the device to be miniature resulting in the implementation of a small battery as the power source.The project builds and simulates an amplifier present in the pacemaker and compares the adiabatic logic with CMOS to identify the power saving.

Keywords: Very Large Scale Integration, Adiabatic Circuits, Pacemaker, Area, Power Reduction, Simulation

Problem Statement and Objective

- There is a gap in the implementation of the proposed adiabatic logic in the bio-medical field such as implantable devices.
- This project aims to bridge the gap between the theory of adiabatic logic in the bio-medical field through an adiabatic design and simulation of an Op-Amp used in Pace.

Methodology

Adiabatic Logic

- Adiabatic circuits work on the principle of charging and discharging based on the clock cycle of the input voltage. The circuit charges power when the clock moves from low to high this phase is the Evaluate phase and discharges when the clock moves from high to low or the Recover phase.
- The logic can be implemented through capacitors or can be enhanced by the addition of CMOS inverters to the existing logic. There are many existing advanced adiabatic concepts such as Positive Feedback Adiabatic Logic (PFAL) and Efficient Charge Recovery Logic (ECRL)

General Adiabatic Circuit Logic

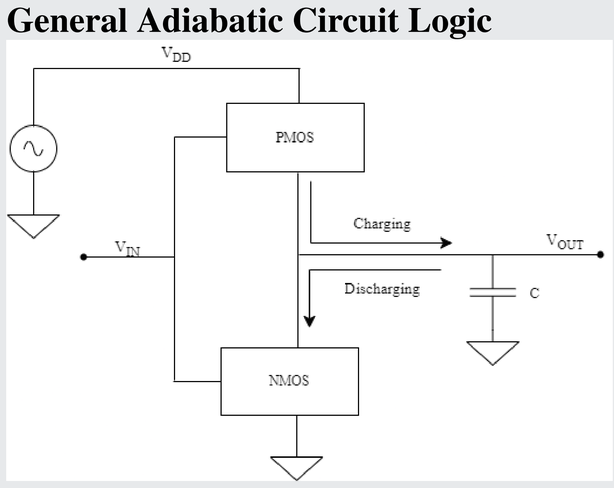

Figure 1: Adiabatic Circuit Logic

Operation of an Adiabatic System

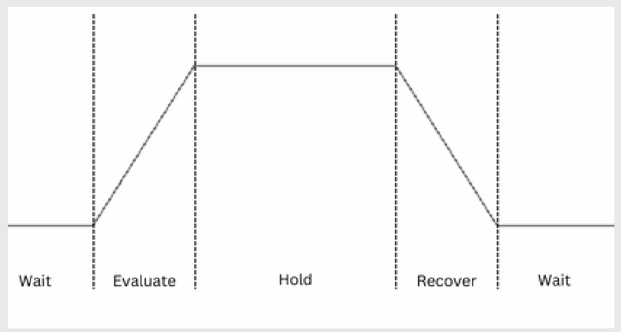

Figure 2: Supply Voltage Waveform of Adiabaic Cirucits

Design

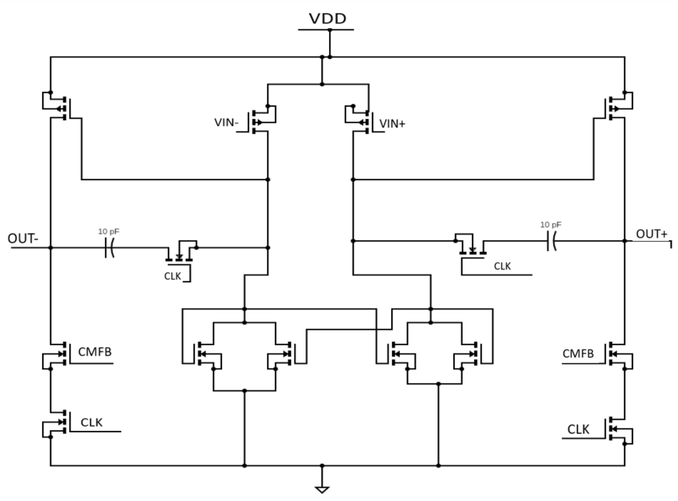

Figure 3: General Switched Op-Amp Circuit used in Pacemakers

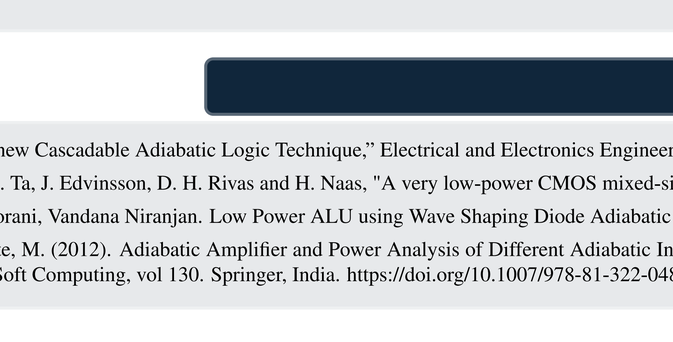

Figure 4: Switched Op-Amp using ECRL Adiabatic Logic

Simulation

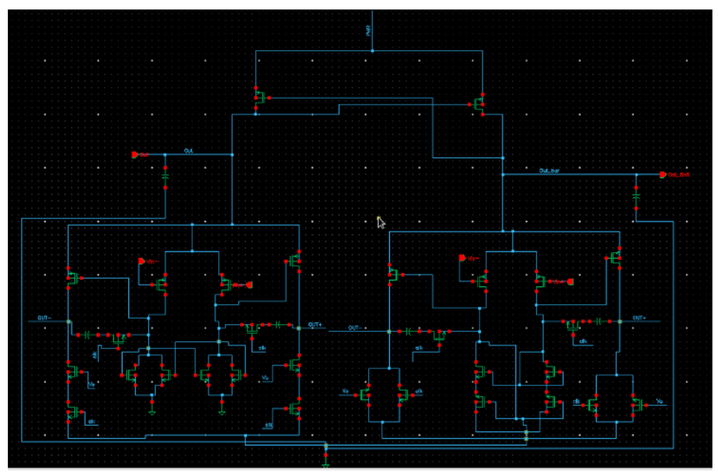

Figure 5: Adiabatic Op-Amp Implemented in Cadence Virtuoso

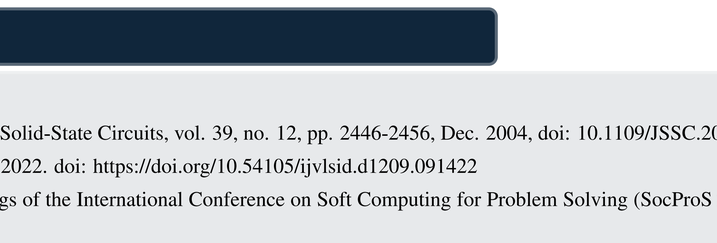

Figure 1: Resultant Waveform of the Designed Circuit

Results and Conclusion

- The waveform obtained from the simulation matches the theoretical output showing the occurrence of evaluation and recovery
- The adiabatic method showed an 18% better efficiency than the conventional CMOS model.
- This implementation can be further developed by involving other parts of the pacemaker and performing a higher complexity implementation of the adiabatic logic.

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