Modeling and Simulation of DFIG Based on FPGA-CPU

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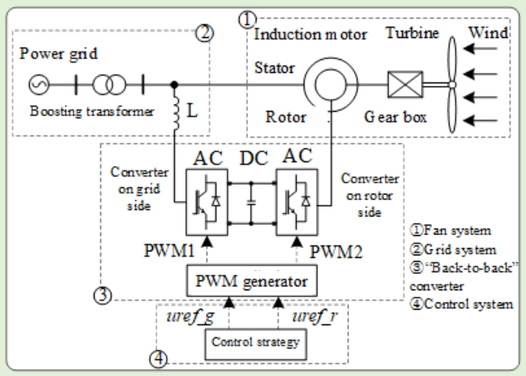
Abstract. In order to realize grid connection and transient real-time simulation of DFIG, a multi-rate parallel real-time simulation method based on co-simulation of Field Programmable Gate Array (FPGA) and CPU is studied. The switching function method is used to model the "back-to-back" converters in the DFIG and optimize the resources, and the modeling segmentation between systems with different step is completed based on PWM averaging to realize multi-rate parallel simulation. The small-step simulation of the "back-to-back" converter is realized with an operational step of 200 by use of high operational rate and strong parallelism of FGPA. Facing the needs of real-time simulation of active distribution network, the 200ns/50 parallel co-simulation of FPGA and independent parallel real-time simulator UREP is realized. By comparing with the off-line simulation results of Simulink and analyzing FGPA resource consumption rate before and after model optimization in this paper, the real-time capacity and accuracy of research method in the paper are verified, which provide a reliable technical support for grid connection and transient research of all kinds of wind power systems.

Keywords: FPGA, DFIG, Real-time simulation

1.Basic structure and simulation step setting of DFIG

As shown in Figure 1, DFIG is mainly composed of four parts: fan, power grid, "back to back" converter and control system. The turbine drives the rotor of the induction motor to rotate through a gearbox. The rotor side is connected to the grid through a "back-to-back" converter, while the stator side is connected directly to the grid. In the figure, parameters respectively represent the modulation voltage of control system on grid side and rotor side, and PWM1 and PWM2 are the trigger pulses of the converters on grid side and rotor side. In the system, the pulse frequency of converter is relatively high, which is generally between thousands of Hertz and tens of thousands of Hertz. In order to obtain higher simulation accuracy, it is necessary to simulate this part with a smaller step. Nevertheless, the simulation scale of system shown in [1] will be severely limited and the simulation time will be increased if the whole system is simulated in small steps. Therefore, the simulation step of "back-to-back" converter is set as 200ns in this paper, and the other part is simulated at 50.

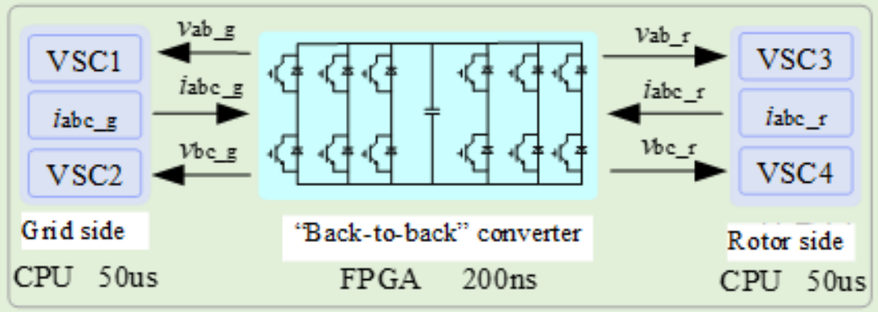


2. FPGA-CPU simulation architecture

Pipeline architecture of FPGA has high parallelism, which is suitable for real-time simulation of small step. With abundant resources and large simulation step, CPU is suitable for large-step simulation of large inertial elements such as fans. As a result, the FPGA-CPU simulation architecture is used to carry out co-simulation of the whole DFIG.

General structure of simulation system

In the simulation system of FPGA-CPU, the entire DFIG is divided into three parts according to different simulation equipment. Among them, PC realizes the development of "back-to-back" converter HDL and initialization of CPU model, FPGA realizes the simulation of "back-to-back" converter with a small step of 200ns, and CPU realizes the operation of fan, external power grid and control signal with a large step of 50. CPU and FPGA realize data communication of large and small steps through Ethernet, and PC monitors the signal to be observed in the CPU model in real time.



3 FPGA modeling and resources optimization of converter

Before co-simulation, it is required to model the "back-to-back" converter running on FPGA, so as to develop HDL. Due to high parallelism and limited resources of FPGA, the repetitive parts of the model can be reduced to save resources.

4 Experimental verification

Based on the previous modeling and optimization methods, this paper selects hardware description language (HDL) to develop the "back-to-back" converter in the DFIG. For xc7k325t in Kintex-7series produced by FPGA for Xilinx company, its package type and pin number is ffg676 and the speed level is -2, which has two Ethernet communication network ports. The input clock of the board is selected as 50MHz, and the 100MHz simulated master clock is generated by doubling the frequency through phase-locked loop (PLL). The simulated CPU is the UREP real-time simulator independently developed by our research group, which has the capacity of 10,000-node power grid scale, millions of kilowatts of new energy, and full electromagnetic transient real-time digital simulation and semi-physical simulation of energy storage equipment. Since the co-simulation of FPGA and UREP has high requirements on real-time performance, this paper chooses the connectionless, fast transmission rate UDP (User Datagram Protocol) as the asynchronous communication protocol. The link between the two is achieved using the ARP protocol before the UDP transport starts.